TITLE 1600G OSFP DR8 Transceivers	DOC No. RFD-20260129100-001	
	REVISION: 01	AUTHORIZED BY: Andy Yang
	DATE: 2026.01.29	CLASSIFICATION: Optics Transceiver

1. Features

- Hot-pluggable 1600G OSFP DR8 form factor
- Compliant with OSFP MSA, close top housing
- Compliant with CMIS Rev 5.2
- Built-in DDMI function
- Silicon photonics MZM solution
- 8x106.25GBd PAM4 electrical and optical interface
- Maximum link length of 500m G.652 SMF fiber
- Single 3.3V power supply
- Operating case temperature 0°C to +70 °C
- Power dissipation < 25W
- Dual MPO-12 APC receptacles
- Compliant with RoHS 2.0

2. Product Applications

- Data center and cloud networks
- 1600G Ethernet and InfiniBand XDR
- Support applications: 1x1600G,2x800G,4x400G, 8x200G

3. Product Description

3.1 Product Name
1600G OSFP DR8

JPC PN	Data Rate	Wavelength (nm)	Distance	Media	Power (dBm)	Sen. (dBm)	Connector	Tem.
P5930DTKCBS5-1	1600G	1311	500m	SMF	-3.3 ~ 4	-.3.4	MPO-12 APC	C

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3.2 Mechanical Specifications

Unit mm

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Optical interface arrangement

The optical port is dual MPO-12 APC connector, with fiber lane assignments as shown in Figure 5.

Figure 5 Optical interface arrangement.

4. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc	-0.3	-	3.6	V	
Storage Temperature	T_s	-40	-	+85	°C	
Operating Humidity	RH	5	-	+95	%	1
Control Input Voltage	VI	-0.3	-	VCC+0.3	V	
RX damage threshold, each Lane	-	5	-	-	dBm	

Note:1 No condensation

5. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0	-	70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	P_{diss}	-	-	25	W	
Supply Current	Icc	-	-	8	A	
Pre-FEC Bit Error Ratio	-	-	-	$2.4x10^{-4}$	-	
Post-FEC Bit Error Ratio	-	-	-	$1x10^{-12}$	-	1
Link Distance (G.652 SMF)	-	2	-	500	m	2

Note:
1. FEC provided by host system
2. FEC required on host system to support maximum distance

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6. Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate,each Lane	-	Gbaud	106.25 ± 100 ppm			
Modulation Format	-	-	PAM4			
Single-Ended Voltage Tolerance	-	mV	-400	-	1400	
Amplitude Tolerance	-	mV	-	-	1000	
Differential Termination Mismatch	-	%	-	-	10	
DC Common-Mode Voltage Tolerance	-	mV	-50	-	1050	
Receiver						
Signaling Rate,each Lane	-	Gbaud	106.25 ± 100 ppm			
Modulation Format	-	-	PAM4			
Differential Output Voltage Peak to Peak	Vout,ppd	mV	-	-	1200	
Differential Termination Mismatch	-	%	-	-	10	
DC Common-mode Voltage Tolerance	-	mV	-50	-	1050	

7. Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate,each Lane	-	Gbaud	106.25 ± 100 ppm			
Modulation Format	-	-	PAM4			
Center Wavelength	λc	nm	1304.5	1311	1317.5	
Side-mode Suppression Ratio	SMSR	dB	30	-	-	
Average Launch Power, each Lane	TxAOP	dBm	-3.3	-	4	1
Outer Optical Modulation Amplitude, (OMAouter), each Lane	OMA	dBm	-0.3	-	4.2	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ	dB	-	-	3.4	
Extinction Ratio, each lane	ER	dB	3.5	-	-	
Transmitter overshoot and undershoot	-	%	-	-	22	
Transmitter power excursion	-	dBm	-	-	2.3	

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Average Launch Power of OFF Transmitter, each lane	TOFF	dBm	-	-	-15	
$RIN_{21.4}OMA$	RIN	dB/Hz	-	-	-136	
Optical Return Loss Tolerance	ORL	dB	-	-	21.4	
Transmitter reflectance	-	dB	-	-	-26	2
Receiver						
Signaling Rate,each Lane	-	Gbaud	106.25 ± 100 ppm			
Modulation format	-	-	PAM4			
Receive Wavelength Range	λc	nm	1304.5	1311	1317.5	
Average Receive Power, each lane	RxAOP	dBm	-6.3	-	4	
Receive Power (OMAouter), each Lane	RxOMA	dBm	-	-	4.2	
Receiver sensitivity (OMAouter), each lane for TECQ < 0.9 dB for 0.9 dB≤TECQ≤SECQ	SENOMA	dBm	-	-	-3.4 -4.3+TECQ	3
Receiver Reflectance	-	dB	-	-	-26	
LOS Assert	LOS_{Ast}	dBm	-	-	-15	
LOS De-Assert	$LOS_{De\text{-}Ast}$	dBm	-	-	-9	
LOS Hysteresis	LOS_{Hys}	dB	0.5	-	-	

Note:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. Pre BER = $6.4E^{-5}$ at TP3.

8. Digital Diagnostic Specifications

Parameter	Symbol	Unit	Min	Max	Notes
Temperature monitor absolute error	DMI_Temp	degC	-3	3	Temperature range 0 to 70°C
Supply voltage monitor absolute error	DMI _VCC	V	-0.1	0.1	Voltage range 3.135 to 3.465V
Channel TX power monitor absolute error, each lane	DMI_TX_Ch	dB	-3	3	Tx power range -3.3 to 4dBm
Channel Bias current monitor, each lane	DMI_Ibias_Ch	mA	-10%	10%	Ibias range 80 to 480mA
Channel RX power monitor absolute error, each lane	DMI_RX_Ch	dB	-3	3	Rx power range -6.3 to 4dBm

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9. Pin Assignment

Figure 1. OSFP Contact Assignment

The notes in the below table are referred to OSFP MSA Specification.

Pin#	Symbol	Description	Logic	Direction	Plug Sequnce
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1

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11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Inverted	CML-I	Input from Host	3
60	GND		Ground		1

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Figure 2, INT/RS Tn circuit

Figure 3 LPWn/PRSn circuit

Recommended Interface

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Memory Map

Compatible with CMIS rev 5.2.

10. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026.01.29	Andy Yang	Mike Sun